

**IF YOU WORK WITH US ONCE,
YOU ARE GOING TO WORK AGAIN!**

FPGA Programming with VHDL

Training Program #1



	DAY1	DAY2	DAY3	DAY4	DAY5
Morning	Binary Logic Intro to VHDL	FPGA Architecture	Sequential Logic Finite State Machines	FPGA Configuration	FPGA Memories
Lunch	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover
Afternoon	VHDL Properties FPGA Primitives & Macros	VIVADO IDE Combinational Logic	Static Timing Analysis	Verification Methods TCL Scripting	FPGA Arithmetic & DSP & Fixed/Floating Point Arithmetic

Trainee Profile:

- Engineers or candidate engineers, working or soon be working on digital design and FPGA field
- Managers, HW design, SW design, test, system engineers etc. who work on FPGA-based systems and want to get knowledgeable about digital design and FPGA field

References (Already took training):



Fundamental VHDL Design & Implementation

Training Program #2



	DAY1	DAY2	DAY3	DAY4	DAY5
Morning	Binary Logic Intro to VHDL	FPGA Architecture	Advanced VHDL Data Types	Static Timing Analysis	Hands-On Design Workshop
Lunch	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover
Afternoon	VHDL Constructs and Coding Principles FPGA Primitives & Macros	Combinational Logic Sequential Logic Finite State Machines	Reusable and Parameterized VHDL Structures	Testbench Development and VHDL Verification	Hands-On Design Workshop

This five-day training program was designed at ASELSAN's request for digital design teams seeking to develop a deeper understanding of VHDL. It shares many topics with Training Program No. 1, but differs significantly in the content covered on Day 3 and during the afternoon session of Day 4.

In the hands-on sessions, the VHDL concepts learned throughout the course are implemented and tested on an FPGA. Typically, after making a design decision together as a class, the design is developed collaboratively and interactively to demonstrate the practical implementation process.

References (Already took training):

aselsan

Fundamentals of FPGA Architecture & Design

Training Program #3



	DAY1	DAY2	DAY3
Morning	FPGA Architecture	Vivado Synthesis Flow	Vivado PaR Flow Timing Closure Techniques
Lunch	Lunch & Recover	Lunch & Recover	Lunch & Recover
Afternoon	FPGA Primitives & Macros VHDL Synthesis Constructs	Static Timing Analysis	Hands-On Workshop

This training focuses on FPGA architecture and the detailed use of AMD Vivado tools. It does not include an in-depth explanation of VHDL. The program was developed in response to a specific request from ASELSAN and is delivered to ASELSAN.

References (Already took training):

aselsan

ZYNQ SYSTEM, HW & SW TRAINING

Training Program #4

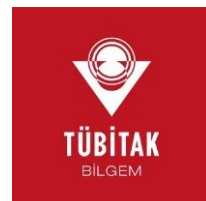


	DAY1	DAY2	DAY3	DAY4	DAY5
Morning	Introduction to Zynq SoC System Architecture & AXI	PS Baremetal SW Design with ARM Cortex A9	Dual Core AMP & PL HW Design with Soft IPs in Vivado	Creating Custom AXI4 Peripherals in PL	DMA & HP AXI Slave Ports
Lunch	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover
Afternoon	Details of PS, PL and Interfaces for Zynq SoC	SW Profiling & Boot & SW Examples	HW Export to Vitis SW Examples	SW Examples for AXI4 Custom Peripherals	HW & SW Examples for DMA

This training focuses on AMD Zynq SoC–based system design, with particular emphasis on the distinction between the Processing System (PS) and Programmable Logic (PL), AXI interfaces, and the development of AXI-compatible IP using both software and VHDL. It also includes practical examples implemented in Vivado and Vitis.

The course covers the software and hardware aspects of Zynq SoC–based designs, the separation and interaction between these domains, and the overall system design approach.

References (Already took training):



Designing with the Zynq UltraScale+ MPSoC

Training Program #5



	DAY1	DAY2	DAY3
Morning	Introduction to Zynq MPSoC System Architecture APU,RPU,GPU,VCU,DPU,PL details	Linux stack options on KV260 Ubuntu vs Petalinux, device tree basics, GStreamer fundamentals	<u>Hands-On</u> : Video scale & video mixer examples, Multi-stream video, picture- in-picture
Lunch	Lunch & Recover	Lunch & Recover	Lunch & Recover
Afternoon	<u>Hands-On</u> : Kria KV260 bring-up boot, SSH/UART & video pipeline basics	<u>Hands-On</u> : Video pipeline with Camera and Display	<u>Hands-On</u> : H.264/H.265 encode & decode using VCU, stream RTSP/UDP, record to file

This training focuses on the AMD Zynq UltraScale+ MPSoC architecture, including the Processing System (PS), Programmable Logic (PL), GPU, DPU, and the connections between these components. It has previously been delivered to teams from TÜBİTAK BİLGEM Gebze.

The course explains which types of applications are best suited for Linux, which functions can be implemented using bare-metal software, and which algorithms can be accelerated in the FPGA fabric. It also includes hands-on exercises covering these different processing domains and their integration within a complete MPSoC-based system.

References (Already took training):



SoC HW & SW Design with MicroBlaze Soft CPU



Training Program #6

	DAY1	DAY2	DAY3	DAY4	DAY5
Morning	Microblaze Intro AXI Protocol	AXI Timer, AXI Interrupt Controller	TEMAC, AXI Ethernet Lite	AXI DMA & AXI- Stream HW Design in Vivado	Creating Custom AXI4 Peripherals in Vivado
Lunch	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover	Lunch & Recover
Afternoon	Vivado & Vitis Intro MIG, AXI Uartlite AXI GPIO, XADC	AXI QSPI, AXI IIC	AXI CAN, AXI Uart 16550	AXI DMA & AXI- Stream SW Design in Vivado	SW Examples for AXI4 Custom Peripherals

This training is similar to Training Program No. 4; however, AMD's MicroBlaze soft processor is used as the CPU. It has previously been delivered to QUBITRIUM.

References (Already took training):



FPGA Timing Analysis, Constraints and Timing Closure

Training Program #7



	DAY1	DAY2	DAY3
Morning	FPGA Timing Overview Digital Timing Concepts	XDC/SDC Timing Constraints	RTL Level Timing Closure Techniques
Lunch	Lunch & Recover	Lunch & Recover	Lunch & Recover
Afternoon	Timing Paths Static Timing Analysis	Clock Domain Crossing - CDC	Vivado Synthesis & Implementation Techniques

This three-day training program was developed at ROKETSAN's request and focuses entirely on FPGA timing topics.

References (Already took training):  **roket**san