

OVERVIEW

The **CAN Controller IP Core** is a synthesizable VHDL design that implements a complete Controller Area Network (CAN) 2.0A/2.0B compliant controller for **FPGA-based** systems. The same field-proven protocol core is available in two integration variants:

- **FIFO variant:** communicates with the user logic via a **FIFO style** interface.
- **AXI CAN variant:** adds a 32-bit **AXI4-Lite** register interface and is designed as a register- and interrupt-compatible replacement for the **AMD LogiCORE IP AXI CAN v1.03.a (DS791)**. It is delivered as a **Vivado IP Integrator** package and runs with the unmodified AMD XCan bare-metal driver.

FEATURES

Protocol core (both variants)

- Compliant with **Bosch CAN** Specification 2.0 Part A and Part B
- Full support for CAN 2.0A (11-bit identifiers) and 2.0B (29-bit identifiers), data and remote frames
- Error handling, error frame generation, error counters, and Error Active/Passive/Bus-Off states
- **Field-proven** on FPGA platforms (AMD/Microchip) through **customer deployments**

FIFO variant

- **Configurable bit timing** via generics (prescaler, SJW, TSEG1, TSEG2, triple sampling)
- Works with external **transmit and receive FIFOs**
- 4 configurable **ID filters** can be set dynamically

AXI CAN variant

- **DS791-compatible register map**, reset values, and access behavior in a 256-byte AXI4-Lite address space
- **Runtime bit timing** through the BRPR/BTR registers
- Configurable **TX and RX FIFOs** (2 to 64 frames) plus a **high-priority TX buffer**
- Up to 4 **acceptance filter** mask/ID pairs for standard, extended, and remote frames
- Configuration, Normal, Sleep (with wake-up), and Loop Back modes
- **12 interrupt sources** on a single interrupt line; ACK, bit, stuff, form, and CRC error status
- Independent AXI and CAN clocks (CAN_CLK 8–24 MHz) with **built-in clock domain crossing**
- **Vivado IP Integrator** package for 7 Series, Zynq-7000, and Zynq UltraScale+ MPSoC devices
- Runs with the unmodified **AMD XCan driver** (v3.11), validated on MicroBlaze

INTERFACE

Figure 1: FIFO variant

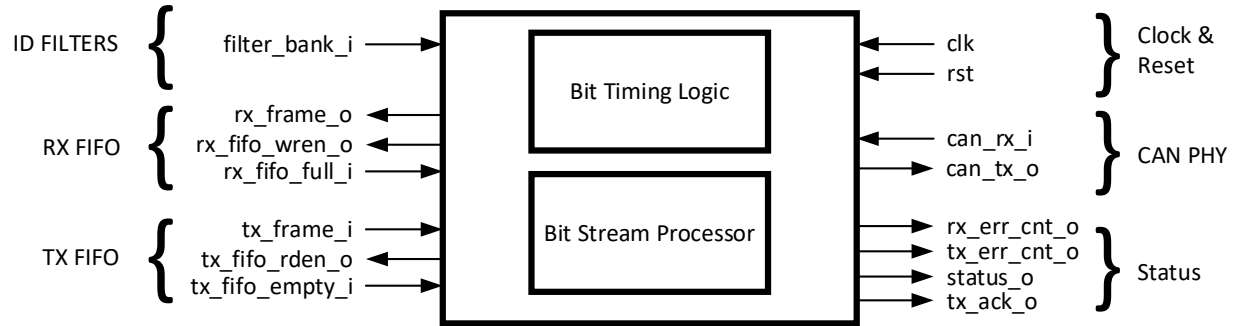
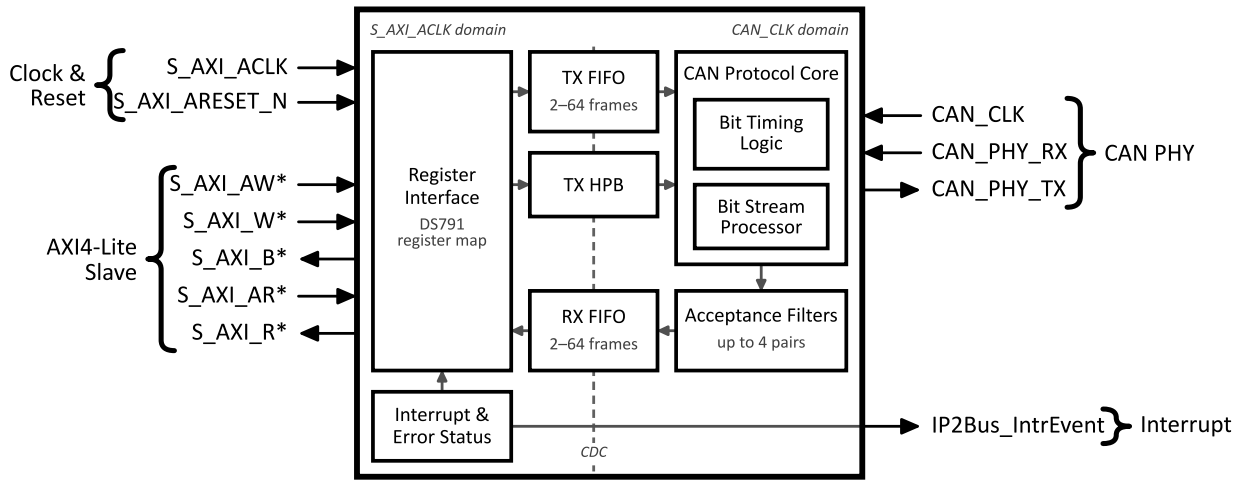


Figure 2: AXI CAN variant (S_AXI_AW*, W*, B*, AR*, R*: AXI4-Lite channel signals)



RESOURCE UTILIZATION

Table 1: Resource Utilization with Default Synthesis Configurations

Variant	Device	Tool	Config.	LUT	FF	LUTRAM	BRAM
FIFO	Microchip PolarFire SoC	Libero SoC v2024.2	–	582	287	–	–
	AMD Artix UltraScale+	Vivado 2023.2	–	400	286	–	–
AXI CAN	AMD Artix-7	Vivado 2025.1	2/2/0	2010	1866	136	0
			4/4/4	2733	3187	136	0
			64/64/4	2885	3251	264	0

PolarFire figures are 4-input LUTs (4LUT) and DFFs. AXI CAN configuration = RX FIFO depth / TX FIFO depth / acceptance filter pairs (2/2/0 is the default); LUT totals include LUTRAM, no DSP blocks are used, and figures include the complete CAN protocol core.

VERIFICATION

- **OSVVM**-based self-checking regression: 30 test cases with over 27,000 checks
- AXI CAN suite passes identically on **GHDL, Questa, and Vivado Simulator**
- Independent compliance model for every DS791 register and reserved address
- All 12 interrupt sources covered; all 5 CAN error types injected at the CAN pins
- **98% line coverage** on the AXI wrapper; CI regression on every change
- Routed Vivado implementation with **timing met at 100 MHz AXI / 24 MHz CAN**

HARDWARE VALIDATION

FIFO variant

- Interoperability with **PCAN-USB, MCP25625, STM32F3DISCOVERY** and **Kvaser USBcan Pro 2xHS v2**
- AMD Artix-7 and Microchip PolarFire SoC platforms at 125 kbit/s, 500 kbit/s, and 1 Mbit/s

AXI CAN variant

Validated on an **AMD Artix-7 (XC7A100T)** with **MicroBlaze** and the AMD XCan driver, a TJA1051 transceiver, and a **PEAK PCAN-USB** node:

- Standard, extended, data, and remote frames in both directions at **125, 250, 500, and 1000 kbit/s**
- Directed tests of FIFOs, high-priority buffer, filters, modes, and interrupts
- **Error Passive, Bus-Off** with automatic recovery, sleep/wake, and reset
- **Stress:** three long-duration runs at 500 kbit/s and 1 Mbit/s, each with 562,500 frames per direction and **zero lost, duplicated, reordered, or corrupted frames**

DELIVERABLES

- **Detailed Integration Guide:** Clock/reset requirements, recommended FIFO selection, bit timing configuration examples, HW validated **Vivado** and **Libero** projects utilizing the IP
- **AXI CAN IP Package:** Vivado IP repository/ZIP with product guide, register map, and DS791 compatibility notes; HW validated **Vivado/MicroBlaze** reference design
- **Verification & Validation Package:** Test summary, functional and code coverage reports, hardware validation evidence (logs/screenshots & live online demo per request)

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