



DSHOT DATA TRANSMITTER IP

General Information

Different communication protocols are used to drive ESCs (Electronic Speed Controllers) in the UAV world. DShot is one of the most common digital communication protocols utilized instead of PWM (Pulse Width Modulation) to drive ESCs.

For simple flight control and navigation purposes, microcontrollers are usually the first choice in the field of UAVs. However, when more advanced features are needed to be deployed on the UAV such as video processing, AI inference with tracking, RF link communication, encryption, video encoding etc. more processing power is needed.

FPGAs and FPGA based SoCs are emerging solutions for UAV flight computers in order to adapt high-speed communication and parallel processing needs of the advanced features. DShot Data Transmitter IP is designed in order to be utilized in FPGA and FPGA based SoC devices to meet the specifications to drive multiple ESCs with DShot digital communication interface

Product Description

DShot Data Transmitter IP transmits speed control information to ESC devices. IP has 2 interface options: Native interface accepts data inputs as standard logic ports and AXI4-Slave interface which communicates with a host CPU such as ARM, NIOS-V or Microblaze through an AXI4-Slave port. Users can use both options according to their needs. C drivers for the host CPU, a demo project both for IP usage in the HW and SW will be provided after the IP is bought.

The IP is highly parameterized and configurable. Number of ESC DShot interface is parametric, so the IP can easily extend to communicate up to 16 ESCs. DShot message frequency can be adjusted to 2/4/8/16/32 kHz, bit rate can be adjusted to support DShot 150/300/600/1200 and duty cycle of logic-1 bit width one encoding of the DShot can be adjusted from 54% to 75% and half of it for logic-0 bit width encoding according to ESC needs during the operation.

DShot Data Transmitter IP is extensively verified in simulation environment and validated with different ESC devices utilized on UAVs. The IP is written in pure VHDL without utilizing any vendor specific macro block, so it can be used in any FPGA or ASIC device.

Features

- Configurable channel number from 1 to 16
- Support of configurable DShot150, DShot300, DShot600 and DShot1200
- Support of configurable 2/4/8/16/32 kHz message frequency (PID frequency) sent to ESC
- Support of configurable 8 different duty cycle adjustment for bit width of logic-1 and logic-0
- Small footprint (~120 LUT for each channel)
- Native (Raw) or AXI4-Lite slave interface options

Native (Raw) Interface Option

Table 1: User Defined Data Types

dshot_ch_inputs	type dshot_ch_inputs is record en : std_logic; arm : std_logic; tm : std_logic; freq : std_logic_vector (1 downto 0); bit_rate : std_logic_vector (2 downto 0); bit_duty : std_logic_vector (2 downto 0); throttle : std_logic_vector (10 downto 0); end record;
t_dshot_ch_input	type t_dshot_ch_input is array (natural range <>) of dshot_ch_inputs;

Table 2: Customizable Parameters

c_num_ch	Number of DShot channels to drive ESCs. <i>Integer</i> data type, up to 16 channels are valid.
c_clk_freq	System clock frequency in Hz. <i>Integer</i> data type.

Table 3: Port Definitions for Native Interface

clk	in	System clock, <i>std_logic</i> type.
rstn	in	Synchronous active-low system reset, <i>std_logic</i> type.
dshot_ch_i	in	DShot input port, <i>t_dshot_ch_input</i> type range (0 to <i>c_num_ch</i> -1).
dshot_tx_o	out	Transmit port for ESC device, <i>std_logic_vector</i> type range (<i>c_num_ch</i> -1 downto 0).
xmit_done_o	out	1 clock logic-1 after each message is delivered to ESC device, <i>std_logic_vector</i> type range (<i>c_num_ch</i> -1 downto 0).

AXI4-Slave Interface Option

User defined data types and customizable parameters are same with the native interface solution.

Table 4: Port Definitions for AXI4-Lite Interface

clk	in	System clock, <i>std_logic</i> type.
rstn	in	Synchronous active-low system reset, <i>std_logic</i> type.
s00_axi_*	-	Standard <i>AXI4-Lite Slave</i> interface with 32-bit data and 6-bit address width
dshot_tx_o	out	Transmit port for ESC device, <i>std_logic_vector</i> type range (<i>c_num_ch</i> -1 downto 0).
xmit_done_o	out	1 clock logic-1 after each message is delivered to ESC device, <i>std_logic_vector</i> type range (<i>c_num_ch</i> -1 downto 0).

Table 5: Register Fields

Field Name	Bit	Type	Description
EN	0	W	Enables DShot transmitting operation when '1'.
ARM	1	W	Transmit 11-bit zero value to indicate ARM when '1'. EN bit must be '1' in order this to be active.
TM	2	W	Value telemetry bit after throttle value in a DShot message.
FREQ	[5:3]	W	Sets transmission frequency of DShot message: 000: 2 kHz 001: 4 kHz 010: 8 kHz 011: 16 kHz 100: 32 kHz 101, 110, 111: Reserved
RATE	[8:6]	W	Sets DShot bit rate: 000: DShot150 001: DShot300 010: DShot600 011: DShot1200 1XX: Reserved
DUTY	[11:9]	W	Sets DShot bit duty cycle of logic-1 and half of it for logic-0: 000: 54% 001: 57% 010: 60% 011: 63% 100: 66% 101: 69% 110: 72% 111: 75%
RESERVED	[15:12]	-	-
THROTTLE	[26:16]	W	11-bit throttle value.
RESERVED	[31:27]	-	-

There are 16 registers, each for independent channel setup. Fields are same for each channel.

Table 6: Registers Table

Channel Name	Register Address
Channel 0	0x00
Channel 1	0x04
Channel 2	0x08
Channel 3	0x0C
Channel 4	0x10
Channel 5	0x14
Channel 6	0x18
Channel 7	0x1C
Channel 8	0x20
Channel 9	0x24
Channel 10	0x28
Channel 11	0x2C
Channel 12	0x30
Channel 13	0x34
Channel 14	0x38
Channel 15	0x3C

Resource Utilization

For AMD 7 series FPGAs with default synthesis options of Vivado 2021.1

Table 7: Resource Utilization for Native Interface

Number of Channels	Number of LUTs	Number of FFs
1	153	145
2	262	269
4	480	517
8	916	1013
16	1724	2005

Table 8: Resource Utilization for AXI4-Slave Interface

Number of Channels	Number of LUTs	Number of FFs
1	354	703
2	464	827
4	689	1075
8	1120	1571
16	1948	2563

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