

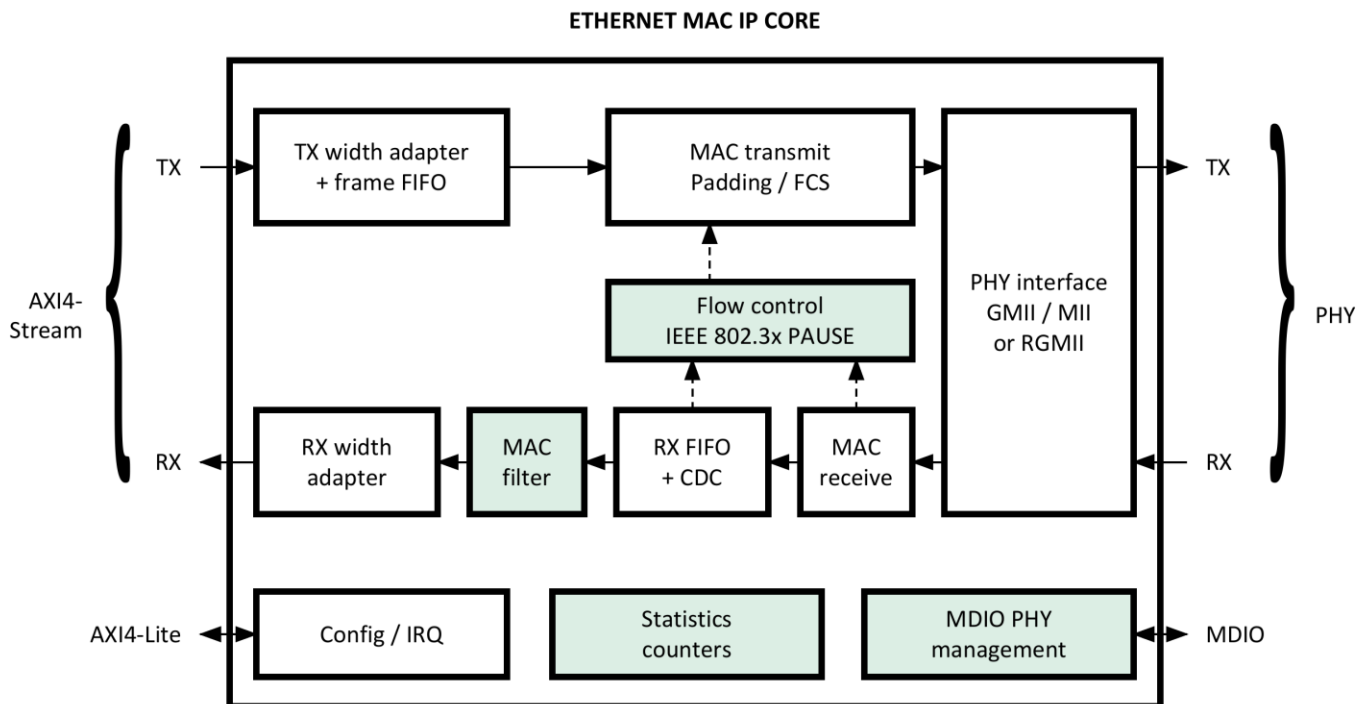
OVERVIEW

The **Ethernet MAC IP Core** connects FPGA user logic to a **10/100/1000 Mbps** PHY through **32-bit AXI4-Stream** data ports and **AXI4-Lite** control registers.

FEATURES

- **GMII/MII and RGMII** PHY options, full duplex and automatic speed detection
- CRC-32/FCS, padding, receive address filtering and maskable interrupts
- Optional **MDIO and statistics; IEEE 802.3x flow control**.

ARCHITECTURE



Green blocks are optional in both GMII/MII and RGMII: flow control (PAUSE_ENABLE), MAC filter (RX_FILTER_ENABLE), MDIO (MDIO_ENABLE) and statistics (STATS_ENABLE). Flow control uses IEEE 802.3x PAUSE frames. Dashed arrows indicate flow control.

Both GMII/MII and RGMII include 4096-byte TX and RX frame FIFOs. TX transmission starts after a complete frame is buffered.

CONFIGURATION AND INTEGRATION

The shared top module selects GMII/MII or RGMII through **PHY_INTERFACE**. Parameters set optional blocks, PHY address and FPGA clock/I/O options. Software controls the station MAC, receive address filtering, TX/RX enables and interrupts.

RESOURCE UTILIZATION

Measured on 22 Sep 2026 with TX/RX frame FIFOs included. Only **MDIO and statistics** vary; RX filtering and flow control stay enabled.

Table 1: AMD FPGA resources, Vivado 2023.2

Device	Interface	MDIO	Statistics	LUT	FF	BRAM
Artix-7	GMII/MII	Enabled	Enabled	1974	2159	4
Artix-7	GMII/MII	Disabled	Disabled	1222	1551	4
Artix-7	RGMII	Enabled	Enabled	1888	1891	2.5
Artix-7	RGMII	Disabled	Disabled	1151	1281	2.5
Kintex UltraScale+	GMII/MII	Enabled	Enabled	1995	2134	4
Kintex UltraScale+	GMII/MII	Disabled	Disabled	1245	1526	4
Kintex UltraScale+	RGMII	Enabled	Enabled	1896	1866	2.5
Kintex UltraScale+	RGMII	Disabled	Disabled	1161	1256	2.5

Artix-7: xc7a100tfgg484-2. Kintex UltraScale+: xcku3p-ffvb676-2-e.

Table 2: PolarFire MPF300TS-1FCG1152I, Libero SoC 2024.2

Interface	MDIO	Statistics	4LUT	DFF	LSRAM	uSRAM
GMII/MII	Enabled	Enabled	3814	2415	6	3
GMII/MII	Disabled	Disabled	2244	1808	6	3
RGMII	Enabled	Enabled	3545	2019	4	0
RGMII	Disabled	Disabled	2013	1419	4	0

VALIDATION AND DELIVERABLES

GMII/MII reference designs: verified on ALINX AX7101 / RTL8211E at 10/100/1000 Mbps. **RGMII** reference design verified on AXKU3 / JL2121D at 10/100/1000 Mbps.

Deliverables include Verilog RTL, integration documentation, synthesis scripts and example Vivado and Libero projects.

For quotations and licensing: info@anadologic.com.