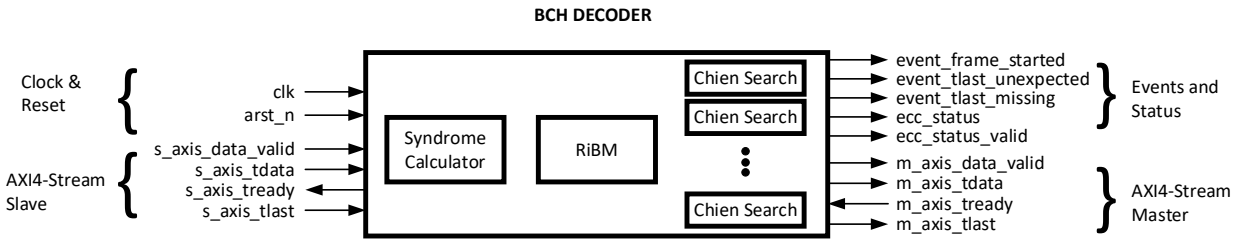
OVERVIEW

The **BCH Encoder/Decoder IP Core** is a synthesizable VHDL design that implements a complete Bose–Chaudhuri–Hocquenghem (BCH) Error Correction Code (ECC) engine for raw **NAND flash** memories. It is designed for integration into **FPGA/SoC-based** NAND flash controllers and targets **ONFI compliant** devices.

FEATURES

- **512-byte** data block length (sector)
- Error correction capability: **t=12**
- Galois Field: **GF(2^{14})**
- ECC redundancy: **t.m = 168 bits** → 21 bytes per 512-byte sector
- Novel decoder architecture via **Reformulated inversionless Berlekamp-Massey (RiBM)**
- **Low resource footprint** and low LUT utilization (< 8000 LUT for logic)
- Industry-standard **AXI4-Stream** interface
- Corrected **error count** and uncorrectable status reported via **status ports**
- **Seamless integration** with ANADOLOGIC's **ONFI NAND Flash Controller** IPs
- **Parametric design** via VHDL package parameters
- Up to **1.6 Gbps** throughput

ARCHITECTURE



DELIVERABLES

- **Detailed Integration Guide:** clock/reset requirements, interface timing, configuration & regeneration flow for BCH parameters, and example integration projects
- **Verification & Validation Package:** test summary, detailed simulation results (including error injection up to t), and hardware validation evidence (logs/screenshots & live online demo per request)

For quotation requests, licensing options, and more information, please contact info@anadologic.com

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